AMENDMENTS TO THE SPECIFICATION

Please amend paragraphs 14, 28, 31, 33-34, 37, 43 and 45 in the specification as shown below:

Paragraph 14 should read:

The method and apparatus further includes a delay circuit operably coupled to the output port of the first flip flop, such that the delay circuit is capable of receiving the flip flop output signal and generating a delayed timing signal. The delay circuit includes one or more delay buffers and a plurality of gates which provide for a delay of the incoming flip flop output signal. The delayed timing signal furthermore may be a time-offset timing signal. The method and apparatus further include[s] at least one clock speed adjusting circuit operably coupled to the delay circuit. Similar to the delay circuit, the clock speed adjusting circuits include delay buffers and various combinations of gates to provide for a specific timing offset.

Paragraph 28 should read:

The apparatus 300 further includes a register 320 operably coupled to receive the delay select signal 142 from the sequencer 304 and the incoming clock signal 110. Disposed between the register 320 and the logic gate 318 is a logic gate flip flop 322, such as a D flip flop. The logic gate flip flop 322 receives the incoming clock signal 110 and timing indicator signal 324 from the logic gate 318.

Paragraph 31 should read:

As recognized by one [have] having ordinary skill in the art, logic gate 318 is illustrated here and as a XOR gate, but may be any other suitable combination of logic gates provided for the indicator 324 which is provided to the logic gate flip flop 322.

Paragraphs 33 and 34 should read:

As illustrated herein, a setup time 404 indicates the transition of the incoming timing signal 110 from a low state to a high state as compared to the corresponding timing signals 122 and lock adjusted signals 134[-40], 136, 138 and 140. In the exemplary illustrated timing

diagram of FIG. 4, it is illustrated that the timing signal 136 corresponds to the incoming clock signal, therefore the apparatus 102 of FIG. 1 would be considered to [the] be operating at a processing speed relative to a 10% delay. Based on the timing diagram of FIG. 4, the timing signals 122 and 134 meet the setup time 404 requirement for the second flip flop 146 of FIG. 1. Timing signals 136, 138 and 140 violate the setup time which indicate that the caused delay is too much and therefore the value on the output of the second flip flop 146, output signal 152, may be wrong.

FIG. 5 illustrates a flow chart representing the steps of a method for determining a processing speed of an integrated circuit. The method begins, step 500, by receiving input signal and an incoming timing signal and a first flip flop to generate a first flip flop output signal, step 502. Similar to the discussion above with regards to FIG. 1, the input signal 106 is received by the first flip flop~~, flip flop~~ 104, as well as the incoming timing signal 110 such that the first flip flop output signal 114 is generated.

Paragraph 37 should read:

The next step of the method, step 516, includes comparing the output timing signal with a control timing signal. As discussed above with regards to FIG. 3, the control timing signal 316 is compared with the output timing signal 152 using, in one embodiment, a logic gate 318. Thereupon, based on the comparison of the output timing signal 152 relative to the control timing signal [318] 316 the processing speed of the integrated circuit may be determined, thereupon the method is complete, step 518. In another embodiment, further method steps may be performed as indicated by reference block A, 520.

Paragraph 43 should read:

When there are no more integrated circuits for determining the processing speed thereof on the [waver] wafer, the next step is removing each of the integrated circuits from the central wafer, step 556. Thereupon, each of the plurality of integrated circuits may be binned based on the recorded processing speed of each integrated circuit, step 558. Thereupon, the method is complete, step 560. The above method improves the binning process for a wafer having a plurality of integrated circuits disposed thereon[.], [Such] such that each of the plurality of

integrated circuits may be tested for a processing speed and effectively distributed or binned relative to its internal processing speed.

Paragraph 45 should read:

It should be understood that the implementation of other variations and modifications of the invention and its various aspects will be apparent to those of ordinary skill in the art, and that the invention is not limited by the specific embodiments described herein. For example, module 200 may be modified to include any number of delay modules effectively increasing the reliability of the output signal 152. It is therefore contemplated to cover by the present invention, any and all modifications, variations or equivalents that fall within the spirit and scope of the basic underlying principles disclosed in the claims herein.